

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

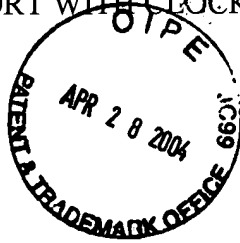
Applicant: Matthew B. Haycock et al.

Title: BIDIRECTIONAL PORT WITH CLOCK CHANNEL USED FOR SYNCHRONIZATION

Docket No.: 884.509US2

Filed: October 21, 2003

Examiner: Daniel Chang



Serial No.: 10/690235

Due Date: May 24, 2004

Group Art Unit: 2819

Commissioner for Patents

P.O. Box 1450


Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ A return postcard.
- ☒ A Response Under 37 C.F.R. 1.111 (5 Pages).
- ☒ A Communication Concerning Related Applications (2 pgs).
- ☒ A Supplemental Information Disclosure Statement (2 pgs.), Form 1449 (1 pg.), and copies of 6 cited documents.
- ☒ Terminal Disclaimer (3 pgs.).
- ☒ Authorization to charge Deposit Account in the amount of \$110 for Terminal Disclaimer Fee and in the amount of \$180.00 to cover the fee for consideration of Information Disclosure Statement under 97(c)

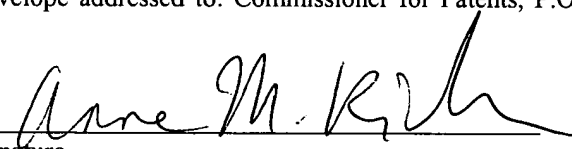
If not provided for in a separate paper filed herewith, Please consider this a **PETITION FOR EXTENSION OF TIME** for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Customer Number 21186

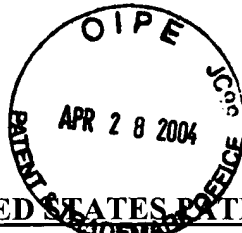
By: 
Atty: John M. Dahl
Reg. No. 44,639

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Anne M. Richards
Name


Signature

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
(GENERAL)



S/N 10/690235

PATENT

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Title: BIDIRECTIONAL PORT WITH CLOCK CHANNEL USED FOR
SYNCHRONIZATION

COMMUNICATION CONCERNING RELATED APPLICATION(S)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
09/644463	August 23, 2000	884.303US1	SIMULTANEOUS BIDIRECTIONAL PORT WITH SYNCHRONIZATION CIRCUIT TO SYNCHRONIZE THE PORT WITH ANOTHER PORT
09/659499 6424175	September 11, 2000	884.307US1	BIASED CONTROL LOOP CIRCUIT FOR SETTING IMPEDANCE OF OUTPUT DRIVER
09/694901 6445170	October 24, 2000	884.333US1	CURRENT SOURCE WITH INTERNAL VARIABLE RESISTANCE AND CONTROL LOOP FOR REDUCED PROCESS SENSITIVITY
09/824370 6448811	April 2, 2001	884.403US1	INTEGRATED CIRCUIT CURRENT REFERENCE
09/835600 6507225	April 16, 2001	884.450US1	CURRENT MODE DRIVER WITH VARIABLE EQUALIZATION
09/951909 6529037	September 13, 2001	884.508US1	VOLTAGE MODE BIDIRECTIONAL PORT WITH DATA CHANNEL USED FOR SYNCHRONIZATION
09/894865	June 28, 2001	884.509US1	BIDIRECTIONAL PORT WITH CLOCK CHANNEL USED FOR SYNCHRONIZATION

COMMUNICATION CONCERNING RELATED APPLICATIONS

Serial Number: 10/690235

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Title: BIDIRECTIONAL PORT WITH CLOCK CHANNEL USED FOR SYNCHRONIZATION

Page 2

Dkt: 884.509US2

09/972327
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October 5, 2001

884.527US1

CURRENT MODE BIDIRECTIONAL PORT
WITH DATA CHANNEL USED FOR
SYNCHRONIZATION

Respectfully submitted,

MATTHEW B. HAYCOCK ET AL.

By Applicants' Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

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Name

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